(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
1 February 2001 (01.02.2001)

PCT

(10) International Publication Number
WO 01/08130 A1

(51) International Patent Classification[7]: G09G 3/36

(21) International Application Number: PCT/EP00/06684

(22) International Filing Date: 13 July 2000 (13.07.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
99202395.2 21 July 1999 (21.07.1999) EP
99203621.0 3 November 1999 (03.11.1999) EP

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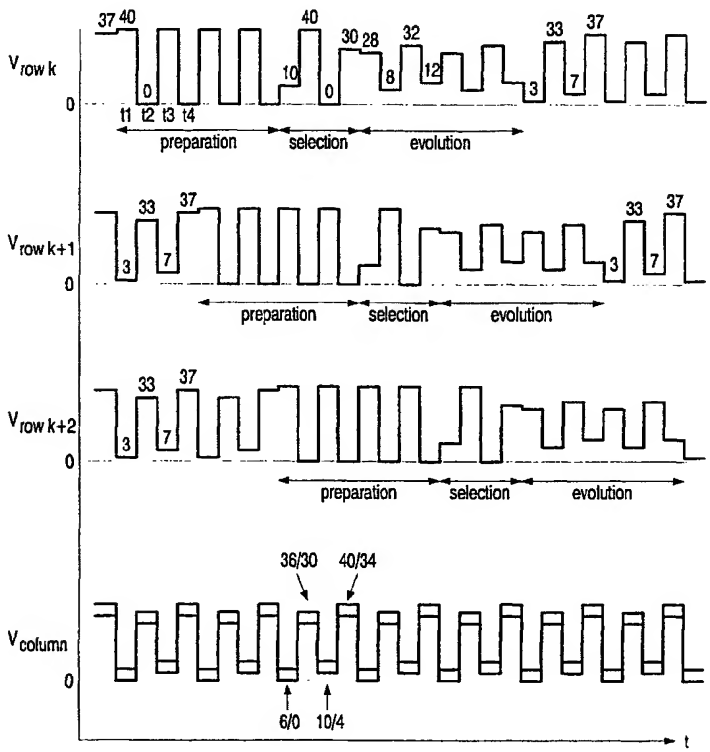
(81) Designated States *(national)*: CN, JP, KR.

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published:
— *With international search report.*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: UNIPOLAR DRIVING OF BISTABLE CHOLESTERIC LIQUID CRYSTAL DISPLAY



(57) Abstract: By adapting the amplitude of pulses in the preparation phase, unipolar driving can be obtained in bistable cholesteric displays, while driving voltages stay within limits of C-MOS technology.

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UNIPOLAR DRIVING OF BISTABLE CHOLESTERIC LIQUID CRYSTAL DISPLAY

The invention relates to a display device comprising a chiral nematic liquid crystal material which is capable of assuming a plurality of states, at least a focal conic state and a planar state of which are stable in the absence of an electric field. Such display devices may be used in, for example, electronic newspapers, GSM telephones, etc.

Such cholesteric liquid crystal displays (CLTC displays) can be driven in a three-phase drive mode. A preparation signal, a selection signal and an evolution signal are consecutively applied to a row electrode. During the selection signal, data signals are presented to the column electrodes which, together with the row electrodes and the intermediate liquid crystal material, define pixels. Such a drive mode is shown in "Dynamic Drive for Bistable Reflective Cholesteric Displays: A Rapid Addressing Scheme", X.-Y. Huang et al, SID 95 Digest, pp. 347-350. In the drive mode shown in this document, the data signals are orthogonal with respect to the evolution and preparation signals (the frequency of the data signal is half that of the evolution and preparation signals), so that the effective value of the evolution and preparation signals is not disturbed by data signals. The relevant mode is rapid but requires high amplitudes of the signals which may be 35 volts, notably in the preparation phase. Since the mode is based on AC drive, a driving circuit to be used must be able to supply the double voltage, i.e. 70 volts. This is too high for the customary IC technologies (CMOS).

It is an object of the present invention to provide a solution to this problem. To this end, a display device according to the invention is characterized in that the display device is provided with drive means for driving the row electrodes with signals from the group of preparation signals, selection signals and evolution signals, and with drive means for driving the column electrodes with data signals in conformity with an image to be displayed, the signals from the group of preparation signals, selection signals, evolution signals and data signals being unipolar with respect to a reference voltage.

As will be described hereinafter, this is possible by adding different auxiliary voltages to all row and column voltages in different units of time. It will then appear that the amplitudes of the signals from the group of preparation signals, selection signals, evolution signals and data signals are defined by the maximally allowable voltages in the drive ICs. This is, for example, not more than 40 (or 50) volts. When zero volt is chosen for the reference voltage, a 40-volt process (or a 50-volt process) may be used for the drive ICs.

These and other aspects of the invention are apparent from and will be elucidated with reference to the embodiments described hereinafter.

In the drawings:

Fig. 1 is a diagrammatic cross-section of a light-modulating cell according to the invention, in two different states,

Fig. 2 shows diagrammatically the voltage/reflection characteristic for the display device of Fig. 1,

Fig. 3 shows a practical embodiment of a display device with a matrix of pixels, and

Figs. 4 to 18 show the variation of the row and column signals for a simplified matrix.

The diagrammatic drawings are not drawn to scale.

Fig. 1 is a diagrammatic cross-section of a part of a light-modulating cell 1 with a chiral nematic liquid crystal material 2 which is present between two substrates 3, 4 of, for example, glass, provided with electrodes 5, 6. If necessary, the device comprises orientation layers 9 which orient the liquid crystal material on the inner walls of the substrates. In this case, the liquid crystal material has a positive optical anisotropy and a positive dielectric anisotropy. In the example of Fig. 1, the light-modulating cell has an absorbing layer 10.

The chiral nematic liquid crystal material 2 is a mixture of a nematic liquid crystal material having a positive dielectric anisotropy and chiral material which is present in such a quantity that a chiral nematic structure results with a given pitch P. This pitch P is the distance across which the directors of the liquid crystal material undergo a rotation of 360 degrees. The liquid crystal molecules are more or less perpendicularly oriented on a wall of the substrate (or in some cases oriented parallel to this wall). A first stable state (the planar

state) now consists of a helix structure having a pitch P (Fig. 1[a]). The thickness d of the light-modulating cell is several times the pitch P (for example, 6 times, but at least 2 times).

The planar state has the property that, of light having a wavelength in a band round $\lambda = n.P$ (n: average refractive index), it reflects that direction of polarization whose polarization rotates with the helix. In the device of Fig. 1, such a liquid is chosen that the planar structure has such a pitch that it reflects, for example, blue light while a black absorbing background 10 has been chosen. Blue characters against a black background (or the other way around) are then generated with the display device shown.

Another stable state which such a chiral nematic liquid crystal material can assume is the focal conic state (Fig. 1[b]) which is produced after the electrodes 5, 6 are energized with one or more electric voltage pulses of a given value (shown by way of a voltage source 11 and a switch 12 in Fig. 1). As it were, the helix structure is broken up into pieces which are arbitrarily oriented and in which incident light is no longer (partly) reflected but can reach the absorbing background.

At a high voltage across the light-modulating cell, the liquid crystal material assumes a third state, referred to as the homeotropic state, i.e. all molecules direct themselves to the field and the light-modulating cell is transparent at all (visible) wavelengths. Dependent on the drive voltage and the switching speed, the light-modulating cell switches from this state to the planar or the focal conic state.

Fig. 2 shows diagrammatically the voltage/reflection characteristic for the display device of Fig. 1. The zero voltage state is dependent on the history. By way of illustration, the planar state is chosen for this purpose, so that the display element reflects blue light with a high reflection value R. For a pulse having an effective value of the (threshold) voltage V_{pf}, the liquid changes over to the focal conic state (curve 1), in which R is substantially zero (the background is visible). When the effective voltage of the pulse is further increased, from V_{off} the reflection increases to a high value. If the liquid is in the focal conic state at 0 volt, the increase of reflection starts at a slightly higher effective voltage V'_{off} (curve 2) and reaches the high reflection at V_{on}. Intermediate reflection levels, which are, however, not unambiguously defined, are possible in the transition range V_{off}-V_{on}. By erasing, as it were, the display device (or a line thereof) prior to each selection (writing information), for example, via the homeotropic state (with one or more pulses), and in the so-called preparation phase, it is achieved that the curves (1), (2) coincide so that V_{off} and V_{on} are unambiguously fixed. V_{off} and V_{on} are defined in this case by the voltage/reflection

characteristic (for example, 1% and 99% of the maximum reflection), but, if necessary, may be defined differently (for example, 5% and 95% of the maximum reflection).

Fig. 3 shows an electrical equivalent of a display device 1 to which the invention is applicable. It comprises a matrix of pixels 18 at the location of crossings of m row or selection electrodes 5 and n column or data electrodes 6. The row electrodes are consecutively selected by means of a row driver 16, while the column electrodes are provided with data via a data register 15. To this end, incoming data signals 21 are first processed, if necessary, in a processor 14. Mutual synchronization takes place via drive lines 17.

The drive of such a display device will be described hereinafter with reference to Figs. 5 to 18. Starting from an AC drive, the signals are rendered unipolar. While this is done with reference to an embodiment with current values for the voltages, a more abstract derivation is given parallel thereto, which relates the drive voltages to the voltages to be maximally used in the drive ICs.

Fig. 4 shows a known drive mode (three-phase drive mode). Preparation signals, selection signals and evolution signals are presented (consecutively) to successive rows (k, k+1, k+2). Data signals which are present at the column electrodes define the picture contents of the relevant row during selection. The frequency of the selection signal and the data signal in Fig. 4 is half that of the evolution and preparation signals. The amplitude of the selection voltage is, for example, $V_{sel} = 7$ V, that of the data voltage $V_{data} = 3$ V, so that the pixel voltage in the "on" state is 10 V and in the "off" state is 4 V. In order that the preparation phase does not last too long (≤ 20 msec), the amplitude in this phase must be $V_{prep} = 35$ V. The amplitude in the evolution phase is, for example, $V_{evol} = 25$ V. A drive IC which drives both rows and columns should have a power supply voltage of at least 70 V so as to be able to generate all these voltages, particularly the peak-to-peak values of the voltage in the preparation phase.

According to the invention, all voltages are rendered unipolar (made positive in this example). The preparation voltage is adapted (see Fig. 5) and is now alternately +37 V, -33 V, +33 V and –37 V (which series is repeated) in the four different units of time t_1, t_2, t_3, t_4. The data voltage may be in phase or in opposite phase with the preparation signal. Dependent thereon, the pixel voltage in the preparation phase is then +40 V, -30 V, +30 V, -40 V in the four different units of time t_1, t_2, t_3, t_4, which corresponds to an effective voltage of 35.35 V, or +34 V, -36 V, +36 V, -34 V, which corresponds to an effective voltage of 35.01 V, which is sufficient to reach the desired reset. In the four different units of time t_1, t_2, t_3, t_4, the following

voltages are added to all rows and columns in a continuous iteration: +3 V, +33 V, +7 V and +37 V, which results in the voltage patterns of Fig. 6. Table 1 shows the values:

Time slot	Added voltage	V_{prep}	V_{sel}	V_{data}	V_{evol}	0-Volt line
t_1	+ 3	+ 40	+ 10	+ 6 / 0	+ 28	+ 3
t_2	+ 33	0	+ 40	+ 36 / + 30	+ 8	+ 33
t_3	+ 7	+ 40	0	+ 10 / + 4	+ 32	+ 7
t_4	+ 37	0	+ 30	+ 40 / + 34	+ 12	+ 37

Table 1

It will be apparent from the Figure and the Table that all drive voltages are now positive and sufficiently low (not more than 40 V) in this example, so that a drive IC can be used which is made by means of a so-called 40-Volt process.

More generally, we can write for the voltages in Table 1:

Time slot	Added voltage	V_{prep}	V_{sel}	V_{data}	V_{evol}
T_1	A_{data}	V_{max}	$A_{sel} + A_{data}$	$2A_{data}$/ 0	$A_{evol} + A_{data}$
T_2	$V_{max} - A_{sel}$	0	V_{max}	$\pm A_{data} + V_{max} - A_{sel}$	$- A_{evol} + V_{max} - A_{sel}$
T_3	A_{sel}	V_{max}	0	$\pm A_{data} + A_{sel}$	$A_{evol} + A_{sel}$
T_4	$V_{max} - A_{data}$	0	$- A_{sel} + V_{max} - A_{data}$	$(V_{max})/ (V_{max} - 2A_{data})$	$- A_{evol} + V_{max} - A_{data}$

Table 1[a]

In this Table:

V_{max} is the maximum power supply voltage of the IC, determined by means of the IC process (for example, 40 volts).

A_{prep} is the minimally required effective value or amplitude (at a square-wave voltage) of the preparation voltage (for example, 35 volts).

A_{sel} is the amplitude of the selection voltage (7 volts in this example).

A_{data} is the amplitude of the data voltage (3 volts in this example).

A_{evol} is the amplitude of the evolution voltage (25 volts in this example).

In the example described above, the frequency of the preparation signal and the evolution signal is twice that of the selection signal. This leads to a high power consumption, notably when writing once, because all row capacitances in the display device must be charged and discharged. This power consumption is decreased when using the signal pattern as is shown in Fig. 7, at which the frequency of the preparation and the evolution signal is half that of the selection signal. To cause the preparation signals on the different rows to be in phase with each other and with the evolution signals, two periods are chosen for the selection signal. The frequency of the preparation signal and the evolution signal is now half that of the previous example (at a given selection time of, for example, 1 msec). The power consumption during preparation and evolution has thus decreased by 50%, but the power consumption during selection has increased by 100%.

Similarly as in the first example, the preparation signal is adapted first, as is shown in Fig. 8. The preparation voltage is thus alternatively +37 V, +33 V, -33 V and –37 V, which corresponds to an effective value of 35.06 V. In the four different units of time t_1, t_2, t_3, t_4, the following voltages are added to all rows and columns in a continuous iteration: +3 V, +7 V, +33 V and +37 V, which results in the voltage patterns of Fig. 9. Table 2 shows the values. All voltages are again between 0 and 40 V.

Time slot	Added voltage	V_{prep}	V_{sel}	V_{data}	V_{evol}	0-Volt line
t_1	+ 3	+ 40	+ 10	+ 6 / 0	+ 28	+ 3
t_2	+ 7	+ 40	0	+ 10 / + 4	+ 32	+ 7
t_3	+ 33	0	+ 40	+ 36 / + 30	+ 8	+ 33
t_4	+ 37	0	+ 30	+ 40 / + 34	+ 12	+ 37

Table 2

By reversing the phase of the selection signal (and also that of the data signal), the voltage jumps at the transition from preparation to selection and at the transition from selection to evolution are reduced, which requires less dissipation. The sequence of different values of the preparation voltage then slightly changes and will be +33 V, +37 V, -37 V, -33 V. The voltages to be added will then be +7 V, +3 V, +37 V and +33 V.

Table 2 can generally be written as follows:

Time slot	Added voltage	V_{prep}	V_{sel}	V_{data}	V_{evol}
t_1	A_{data}	V_{max}	$A_{sel} + A_{data}$	$2A_{data}$/ 0	$A_{evol} + A_{data}$
t_2	A_{sel}	V_{max}	0	$\pm A_{data} + A_{sel}$	$A_{evol} + A_{sel}$
t_3	$V_{max} - A_{sel}$	0	V_{max}	$\pm A_{data} + V_{max} - A_{sel}$	$- A_{evol} + V_{max} - A_{sel}$
t_4	$V_{max} - A_{data}$	0	$- A_{sel} + V_{max} - A_{data}$	$(V_{max})/ (V_{max}-2A_{data})$	$- A_{evol} + V_{max} - A_{data}$

Table 2^a

The power consumption during writing may be further decreased by using only one period of the selection voltage in the selection period. The frequency of the preparation signal and the evolution signal is then a quarter of that of the signal as described with reference to Fig. 4, with a proportionally lower energy consumption, while the energy consumption during writing is the same. The signal pattern is shown in Fig. 10. By causing the phases of the preparation signal at the evolution signal to start alternately with a negative and a positive half period, the preparation signals at the different rows are again in phase with each other and with the evolution signals.

Now, the preparation signal is again adapted first (Fig. 11). The preparation voltage is again alternately +37 V, +33 V, -33 V and –37 V, which corresponds to an effective value of 35.06 V. In the four different units of time t_1, t_2, t_3, t_4, the following voltages are added to all rows and columns in a continuous iteration: +3 V, +7 V, +33 V and +37 V, which results in the voltage patterns of Fig. 12. Table 3 gives the values.

Time slot	Added voltage	V_{prep}	V_{sel}	V_{data}	V_{evol}	0-Volt line
t_1	+ 3	+ 40	+ 10	+ 6 / 0	+ 28	+ 3
t_2	+ 7	+ 40	0	+ 10 / + 4	+ 32	+ 7
t_3	+ 33	0	+ 40	+ 36 / + 30	+ 8	+ 33
t_4	+ 37	0	+ 30	+ 40 / + 34	+ 12	+ 37

Table 3

This Table is identical to Table 2; for the more general formulation, a Table with values which are identical to those of Table 2^a applies. All voltages again remain below the maximally allowable voltages in the drive IC.

By reversing the phase of the selection signal, and hence of the data signal, in all odd rows, the largest voltage jump which occurs at the transition from preparation phase to selection phase (in Fig. 11) is reduced so that the power consumption is further decreased. The sequence of the different values of the preparation voltage then slightly changes and will be +33 V, +37 V, -33 V, -37 V. The voltages to be added will be +7 V, +3 V, +33 V and +37 V.

The examples hitherto particularly relate to writing once. The display of moving images, for example video images, can be effected by means of the signals as shown in Fig. 13. The preparation signal and the evolution signal are now already DC signals (unipolar with respect to 0 volt) which are reversed (presented with an inverse signal) in the next frame. To render all signals unipolar with respect to 0 volt, the preparation signal is adapted as shown in Fig. 14; it alternately acquires the values +37 V and +33 V. In every two consecutive units of time, the values +3 V and +7 V are subsequently added to the row and column voltages. The signals thereby obtained are shown in Fig. 15; the associated voltages are stated in Table 4 and in a more general form in Table 4[a].

Time slot	Added voltage	V_{prep}	V_{sel}	V_{data}	V_{evol}	0-Volt line
t_1	+ 3	+ 40	+ 10	+ 6 / 0	+ 28	+ 3
t_2	+ 7	+ 40	0	+ 10 / + 4	+ 32	+ 7

Table 4

Time slot	Added voltage	V_{prep}	V_{sel}	V_{data}	V_{evol}
t_1	A_{data}	V_{max}	$A_{sel} + A_{data}$	$2A_{data}$/ 0	$A_{evol} + A_{data}$
t_2	A_{sel}	V_{max}	0	$\pm A_{data} + A_{sel}$	$A_{evol} + A_{sel}$

Table 4[a]

For the next frame, the original signals are shown in Fig. 16 and the adapted signals are shown in Fig. 17. The preparation signal alternately acquires the values –37 V and –33 V. In every two consecutive units of time, the values +37 V and +33 V are subsequently added to the row and column voltages (see Fig. 18). The associated voltages are stated in Table 5 and in a more general form in Table 5 [a].

Time slot	Added voltage	V_{prep}	V_{sel}	V_{data}	V_{evol}	0-Volt line
t_3	+ 33	0	+ 40	+ 36 / + 30	+ 8	+ 33
t_4	+ 37	0	+ 30	+ 40 / + 34	+ 12	+ 37

Table 5

Time slot	Added voltage	V_{prep}	V_{sel}	V_{data}	V_{evol}
t_3	$V_{max} - A_{sel}$	0	V_{max}	$\pm A_{data} + V_{max} - A_{sel}$	$- A_{evol} + V_{max} - A_{sel}$
t_4	$V_{max} - A_{data}$	0	$- A_{sel} + V_{max} - A_{data}$	$(V_{max})/ (V_{max} - 2A_{data})$	$- A_{evol} + V_{max} - A_{data}$

Table 5[a]

All voltages now also have an (absolute) value below V_{max} again.

The protective scope of the invention is not limited to the embodiments described. The invention resides in each and every novel characteristic feature and each and every combination of characteristic features. Reference numerals in the claims do not limit the protective scope of the claims. Use of the word "comprise" and its conjugations does not exclude the presence of elements other than those mentioned in the claims. Use of the word "a" or "an" preceding an element does not exclude the presence of a multitude of such elements.

CLAIMS:

1. A display device comprising a chiral nematic liquid crystal material which is capable of assuming a plurality of states, at least a focal conic state and a planar state of which are stable in the absence of an electric field, characterized in that the display device is provided with drive means for driving the row electrodes with signals from the group of preparation signals, selection signals and evolution signals, and with drive means for driving the column electrodes with data signals in conformity with an image to be displayed, the signals from the group of preparation signals, selection signals, evolution signals and data signals being unipolar with respect to a reference voltage.

2. A display device as claimed in claim 1, provided with at least a drive IC, characterized in that the amplitudes of the signals from the group of preparation signals, selection signals, evolution signals and data signals are defined by the maximally allowable voltages in the drive IC.

3. A display device as claimed in claim 1 or 2, characterized in that the amplitude of the signals from the group of preparation signals, selection signals, evolution signals and data signals is not more than 40 volts.

4. A display device as claimed in claim 1, 2 or 3, characterized in that the reference voltage is zero volt.

5. A display device as claimed in claim 1, 2 or 3, characterized in that a preparation signal for a row electrode comprises a plurality of sub-signals of different amplitudes.

6. A display device as claimed in claim 1, 2 or 3, characterized in that an evolution signal for a row electrode comprises a plurality of sub-signals of different amplitudes.

7. A display device as claimed in claim 5 or 6, characterized in that a selection signal for an address electrode comprises a plurality of sub-signals of different amplitudes.

8. A display device as claimed in claim 1, 2 or 3, characterized in that the preparation signals have the same amplitude during a frame period.

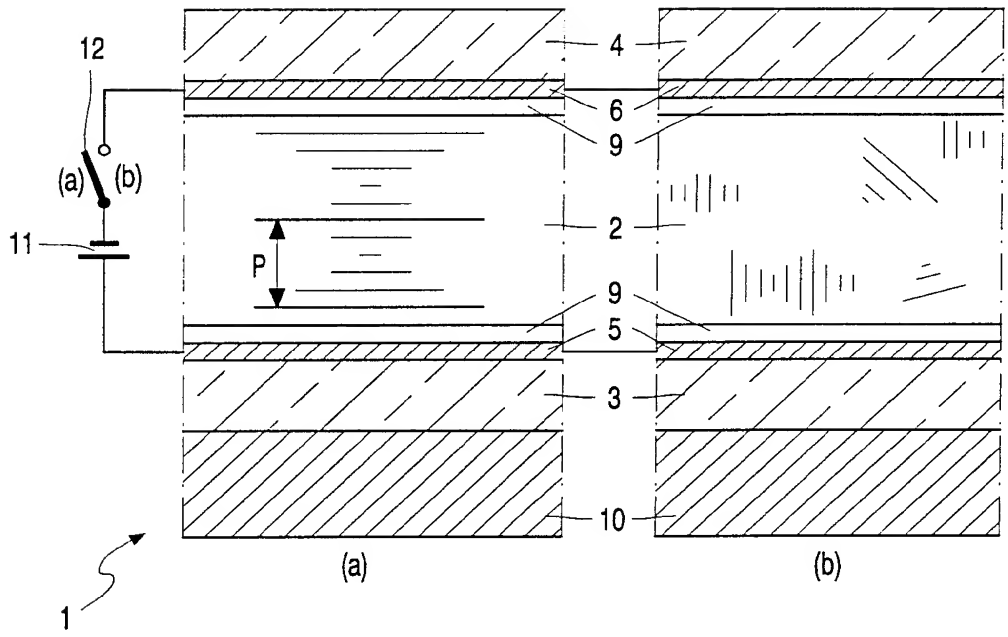


FIG. 1

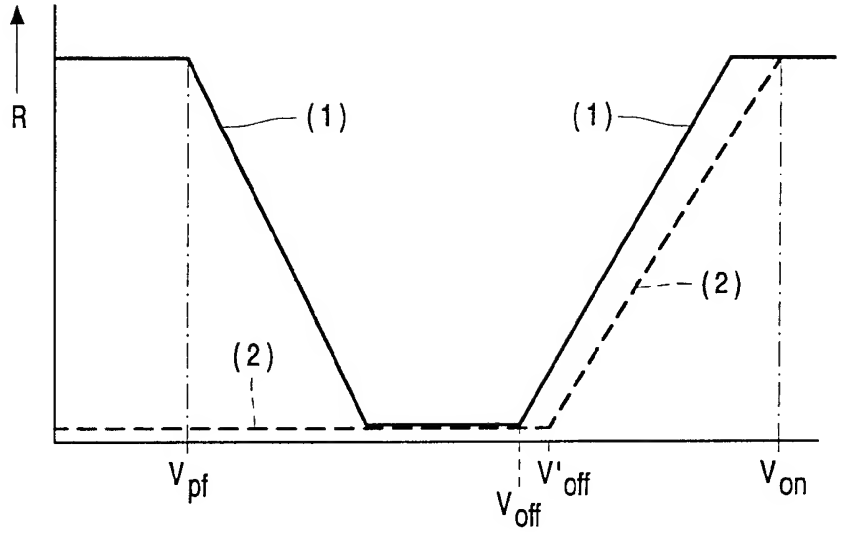
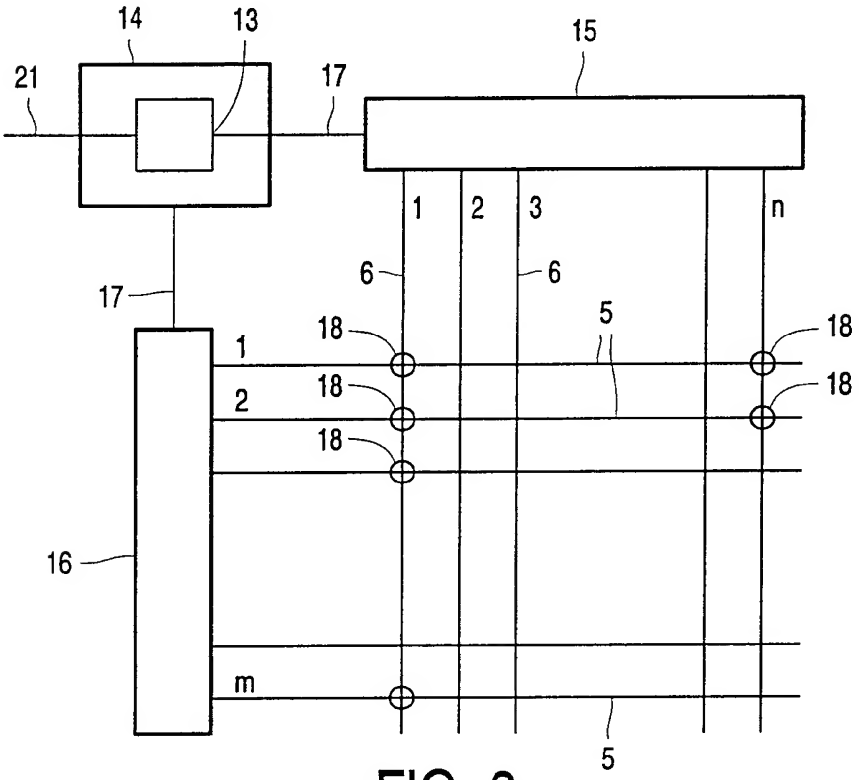

R
(1)
(1)
(2)
(2)
V_{pf}
V_{off}
V'_{off}
V_{on}

FIG. 2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13
15
21
17
17
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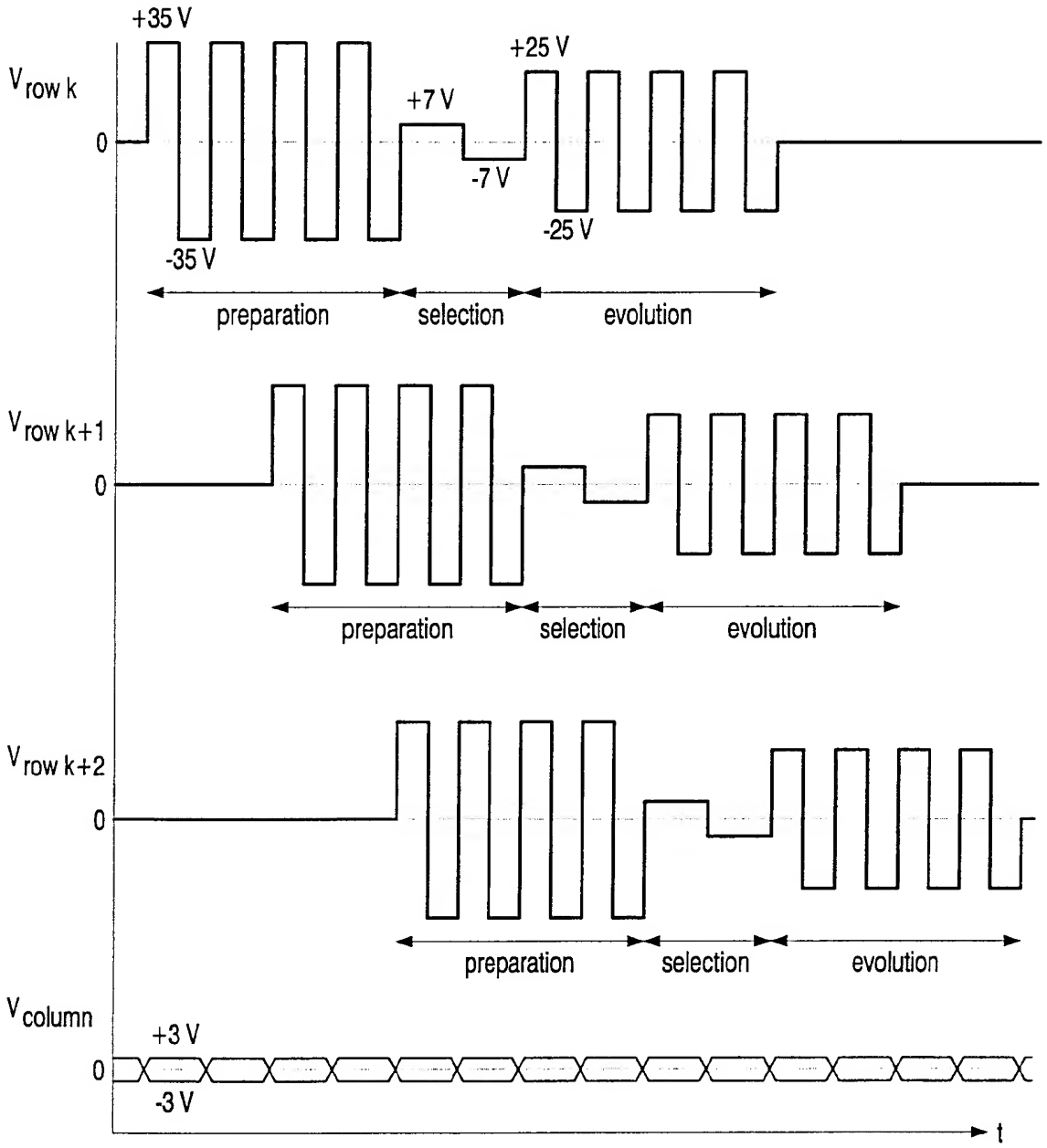
n
6
6
5
18
18
18
18
18
1
2
16
m
5

FIG. 3


+35 V
+25 V
V row k
+7 V
0
-7 V
-25 V
-35 V
preparation
selection
evolution
V row k+1
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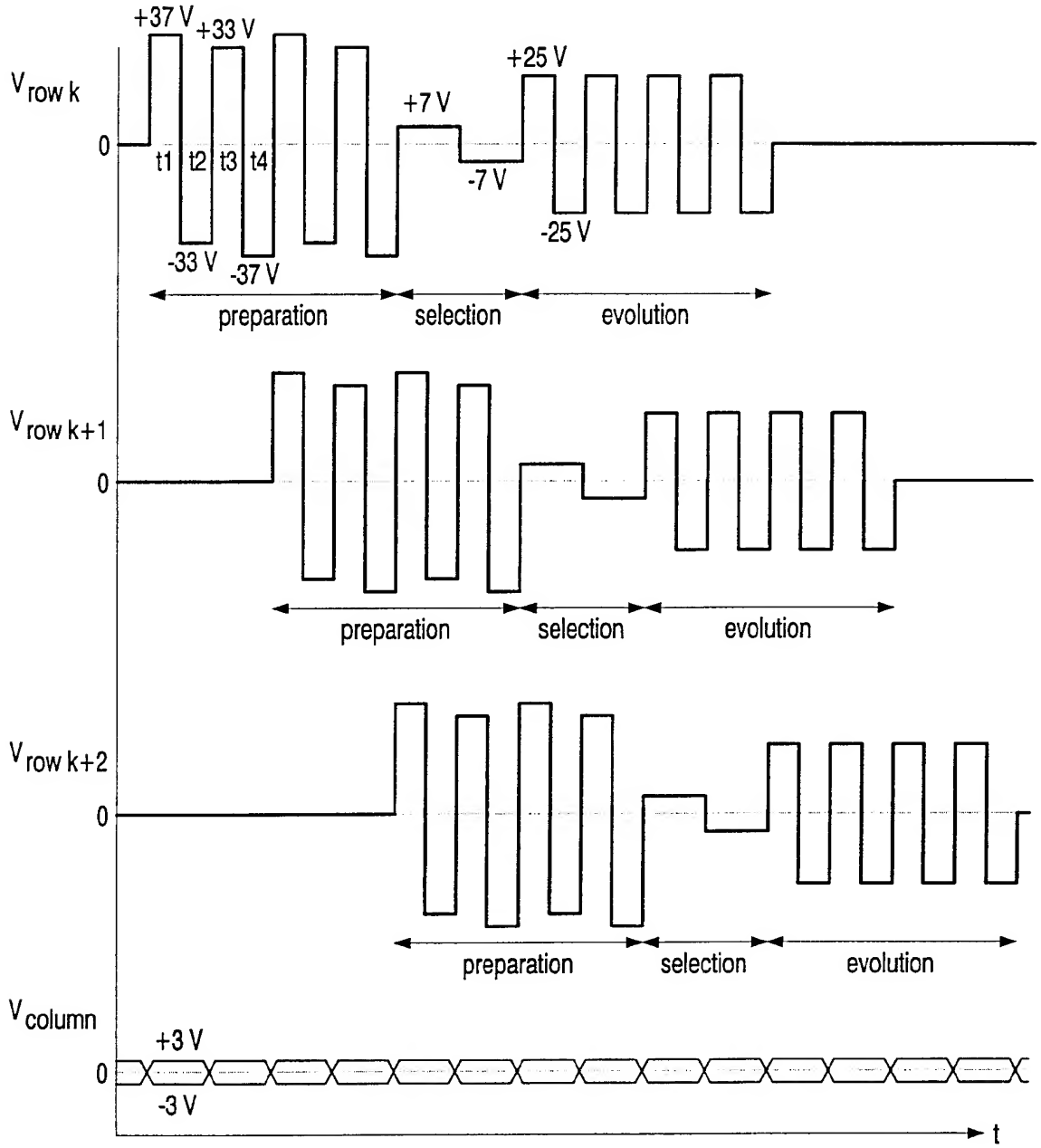
preparation
selection
evolution
V row k+2
0
preparation
selection
evolution
V column
+3 V
0
-3 V
t

FIG. 4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+25 V
V row k
+7 V
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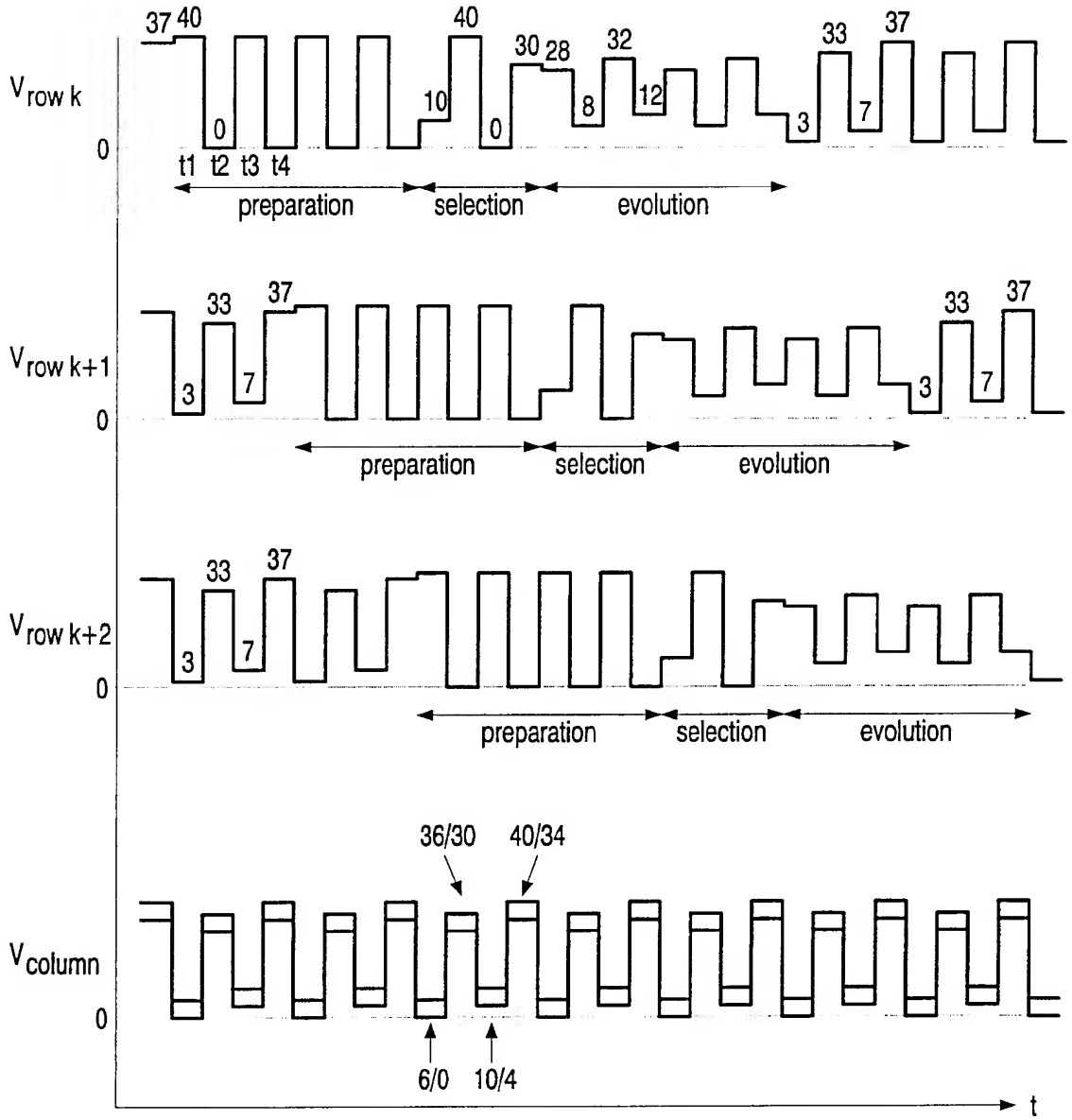
t1
t2
t3
t4
-7 V
-33 V
-37 V
-25 V
preparation
selection
evolution
V row k+1
0
preparation
selection
evolution
V row k+2
0
preparation
selection
evolution
V column
+3 V
0
-3 V
t

FIG. 5


V row k
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37 40
0
40
10
0
30 28
8
32
12
3
33
7
37
t1 t2 t3 t4
preparation
selection
evolution
V row k+1
0
3
33
7
37
3
33
7
37
preparation
selection
evolution
V row k+2
0
3
33
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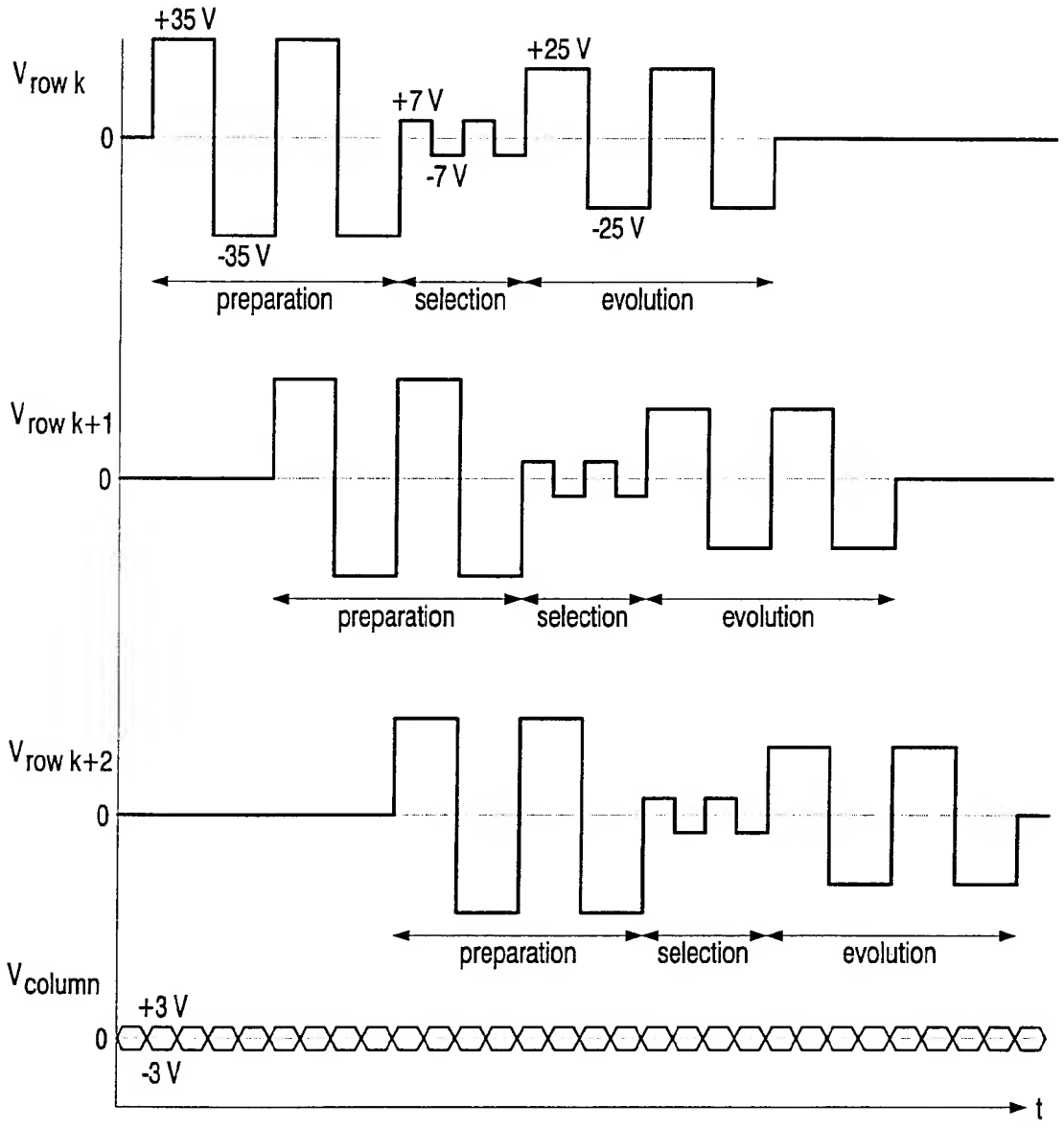
40/34
6/0
10/4
t

FIG. 6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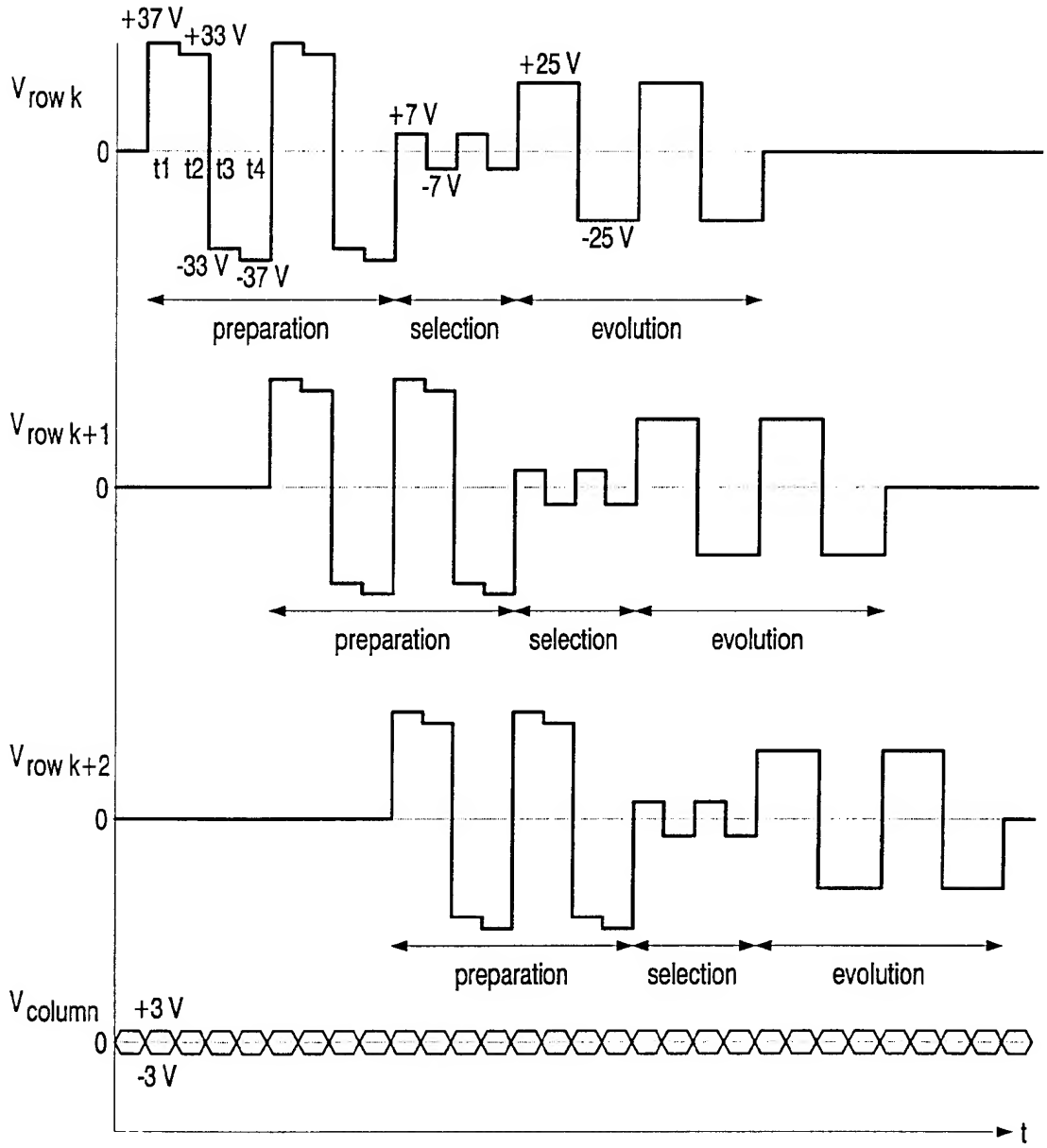
+7 V
-7 V
+25 V
-25 V
-35 V
preparation
selection
evolution
V row k+1
0
preparation
selection
evolution
V row k+2
0
preparation
selection
evolution
V column
+3 V
0
-3 V
t

FIG. 7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0
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preparation
selection
evolution
V row k+1
0
preparation
selection
evolution
V row k+2
0
preparation
selection
evolution
V column
+3 V
0
-3 V
t

FIG. 8

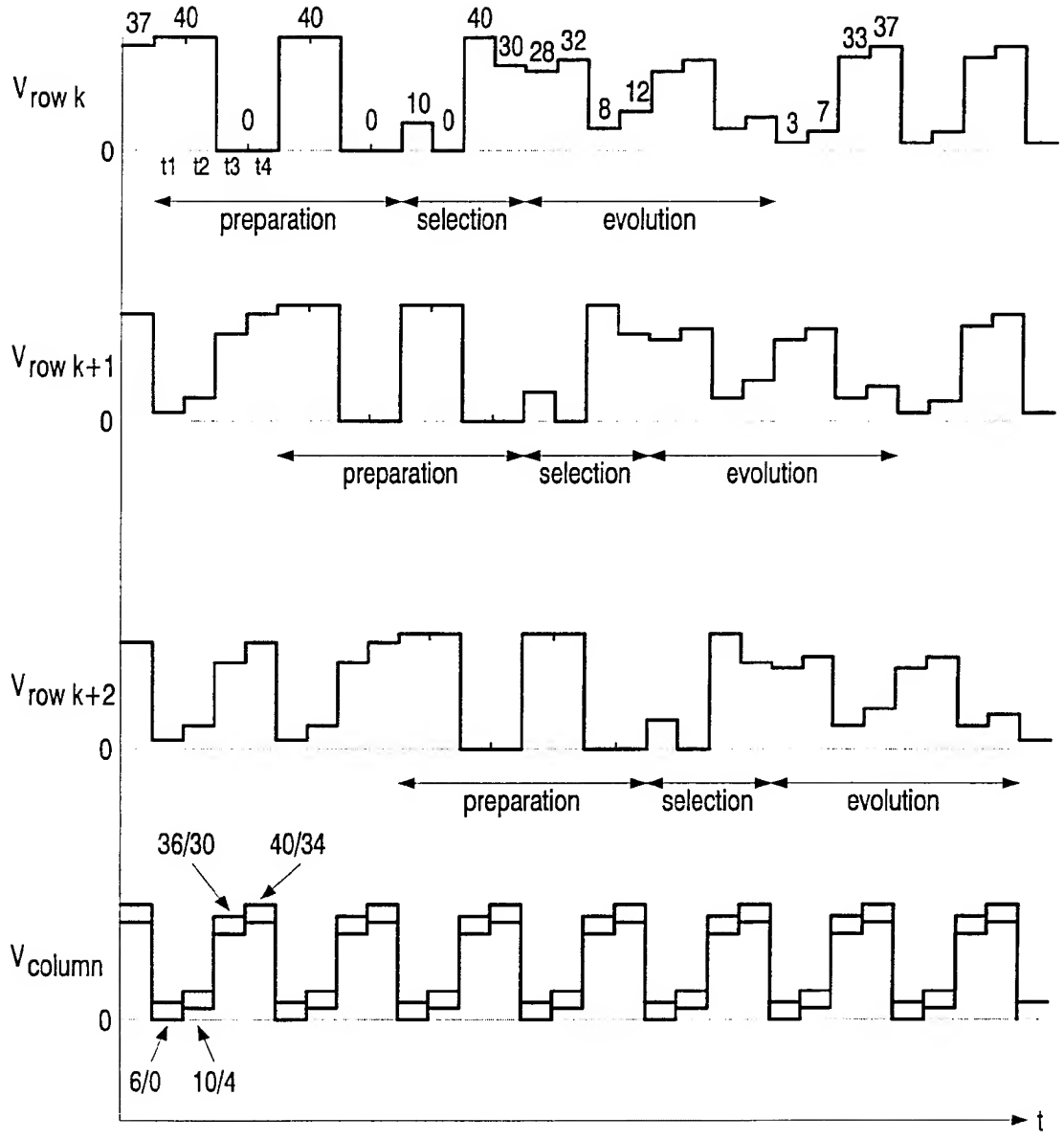
V row k
0
37 40
40
40
30 28 32
33 37
0
10
0
0
8 12
3 7
t1 t2 t3 t4
preparation
selection
evolution
V row k+1
0
preparation
selection
evolution
V row k+2
0
preparation
selection
evolution
36/30
40/34
V column
0
6/0
10/4
t

FIG. 9

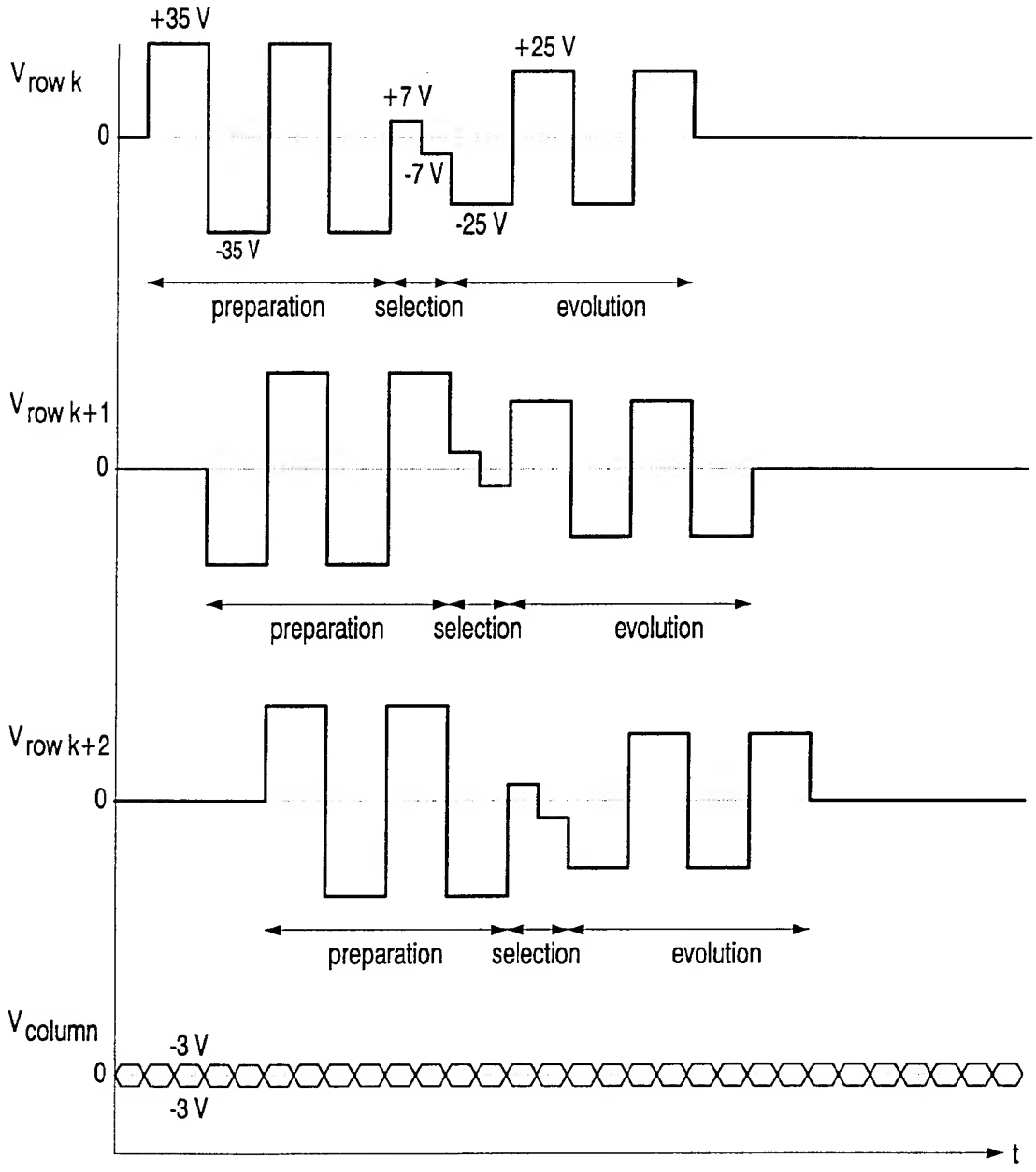
+35 V
+25 V
V row k
+7 V
0
-7 V
-25 V
-35 V
preparation
selection
evolution
V row k+1
0
preparation
selection
evolution
V row k+2
0
preparation
selection
evolution
V column
-3 V
0
-3 V
t

FIG. 10

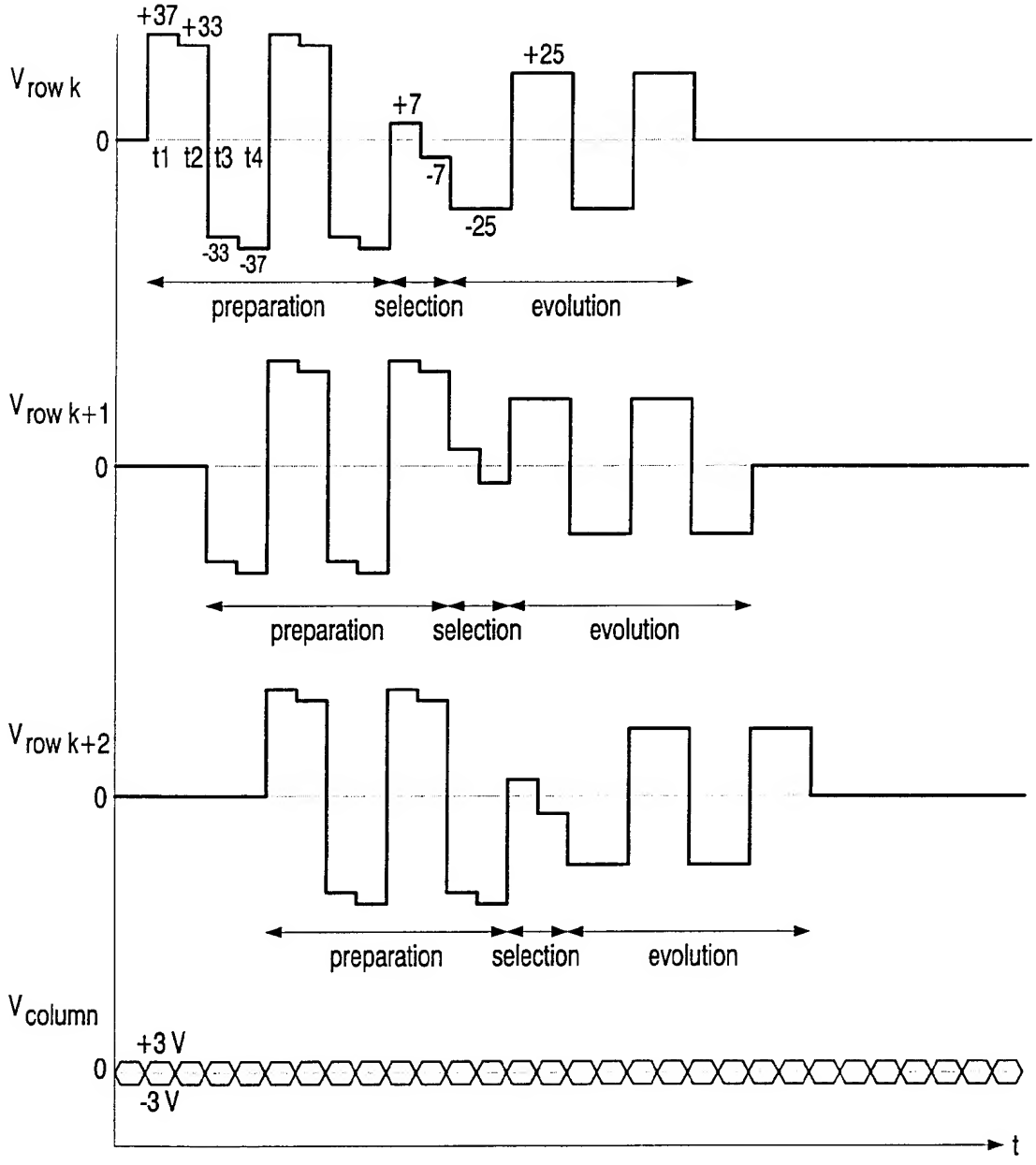
+37
+33
+25
V row k
+7
0
t1 t2 t3 t4
-7
-25
-33
-37
preparation
selection
evolution
V row k+1
0
preparation
selection
evolution
V row k+2
0
preparation
selection
evolution
V column
+3 V
0
-3 V
t

FIG. 11

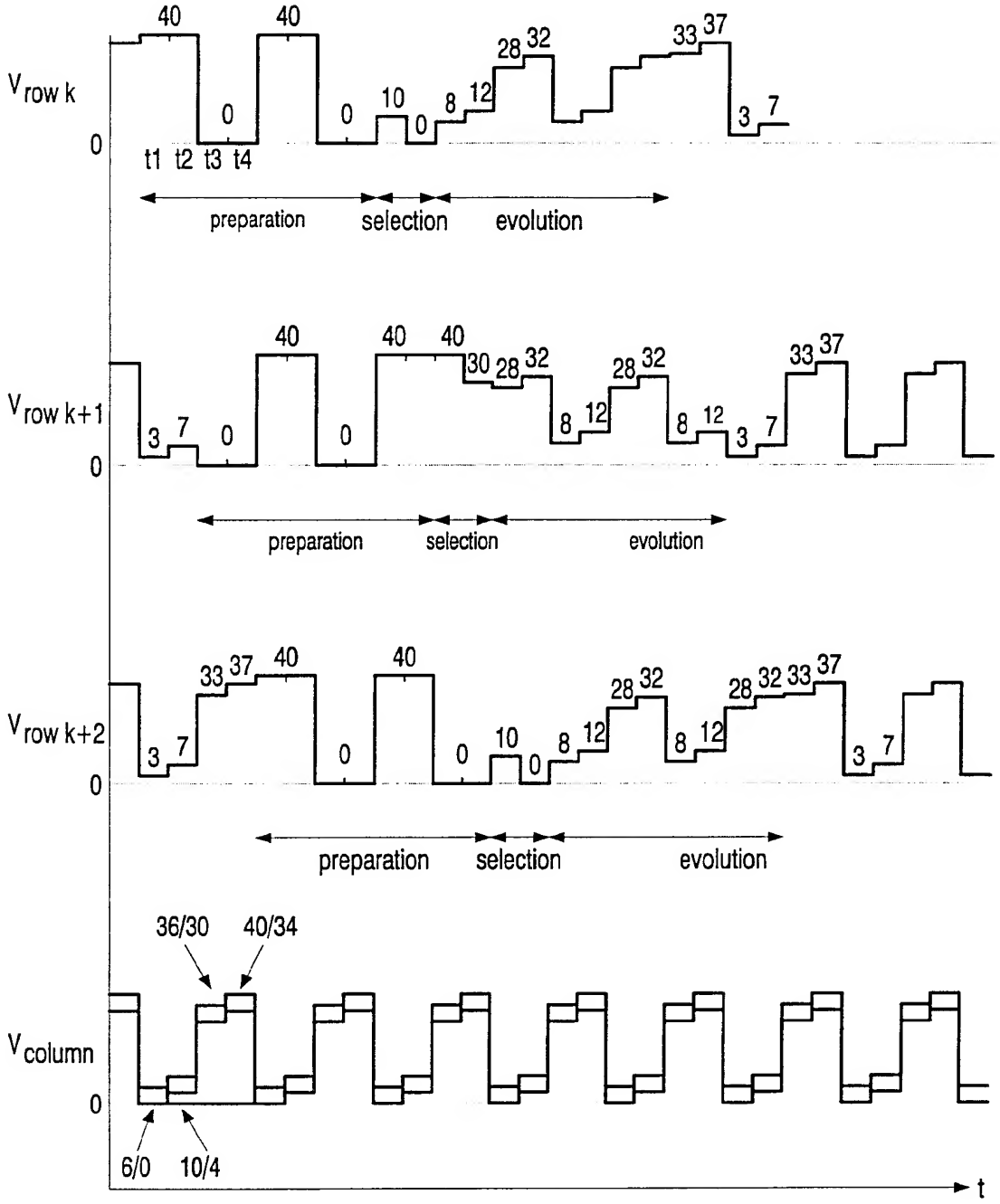
V row k
0
40
40
0
0
10
0
8
12
28
32
33
37
3
7
t1 t2 t3 t4
preparation
selection
evolution
V row k+1
0
3
7
0
40
0
40
40
30
28
32
8
12
28
32
8
12
3
7
33
37
preparation
selection
evolution
V row k+2
0
3
7
33
37
40
0
40
0
10
0
8
12
28
32
8
12
28
32
33
37
3
7
preparation
selection
evolution
V column
0
36/30
40/34
6/0
10/4
t

FIG. 12

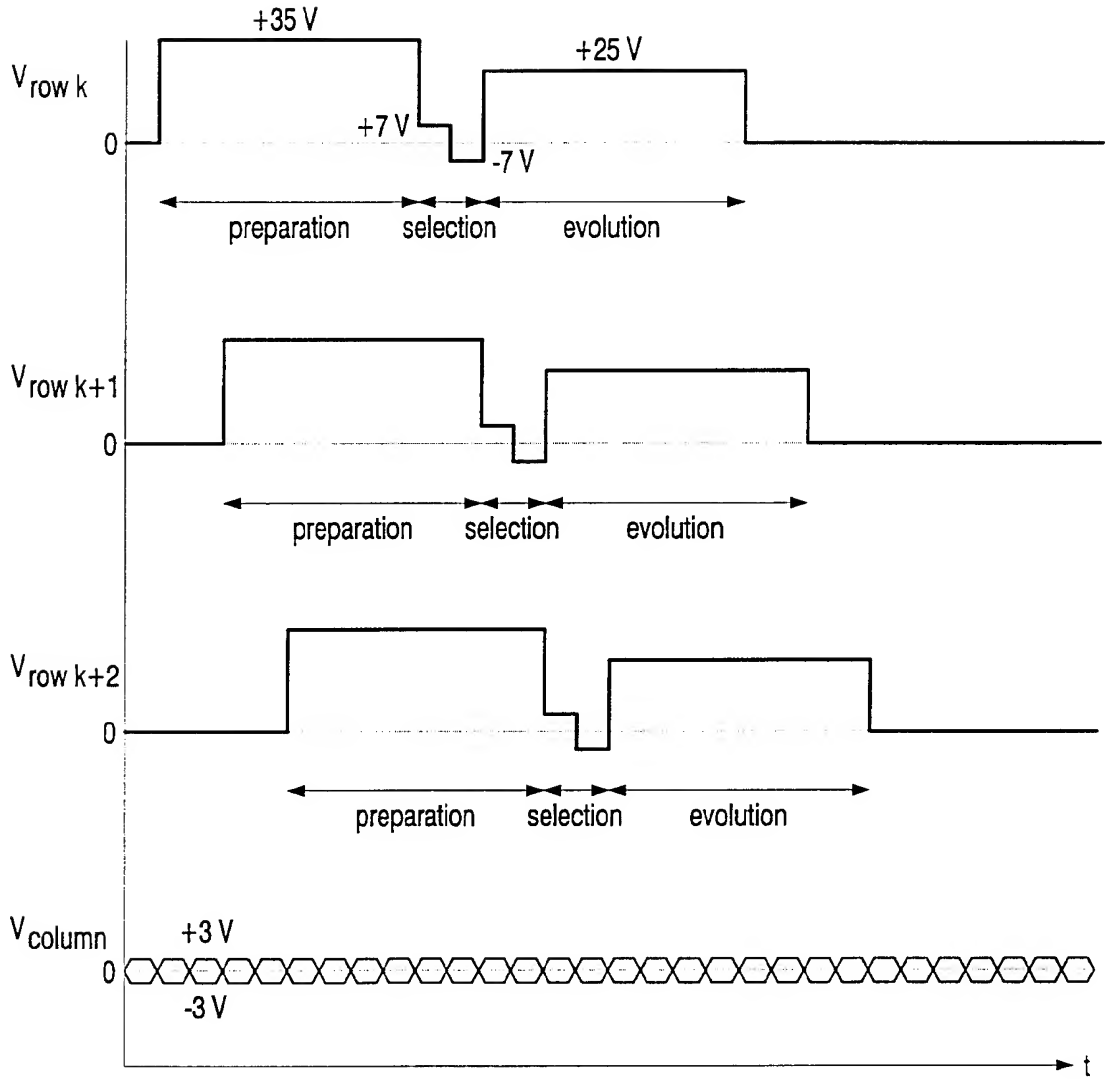
+35 V
+25 V
V row k
+7 V
0
-7 V
preparation
selection
evolution
V row k+1
0
preparation
selection
evolution
V row k+2
0
preparation
selection
evolution
V column
+3 V
0
-3 V
t

FIG. 13

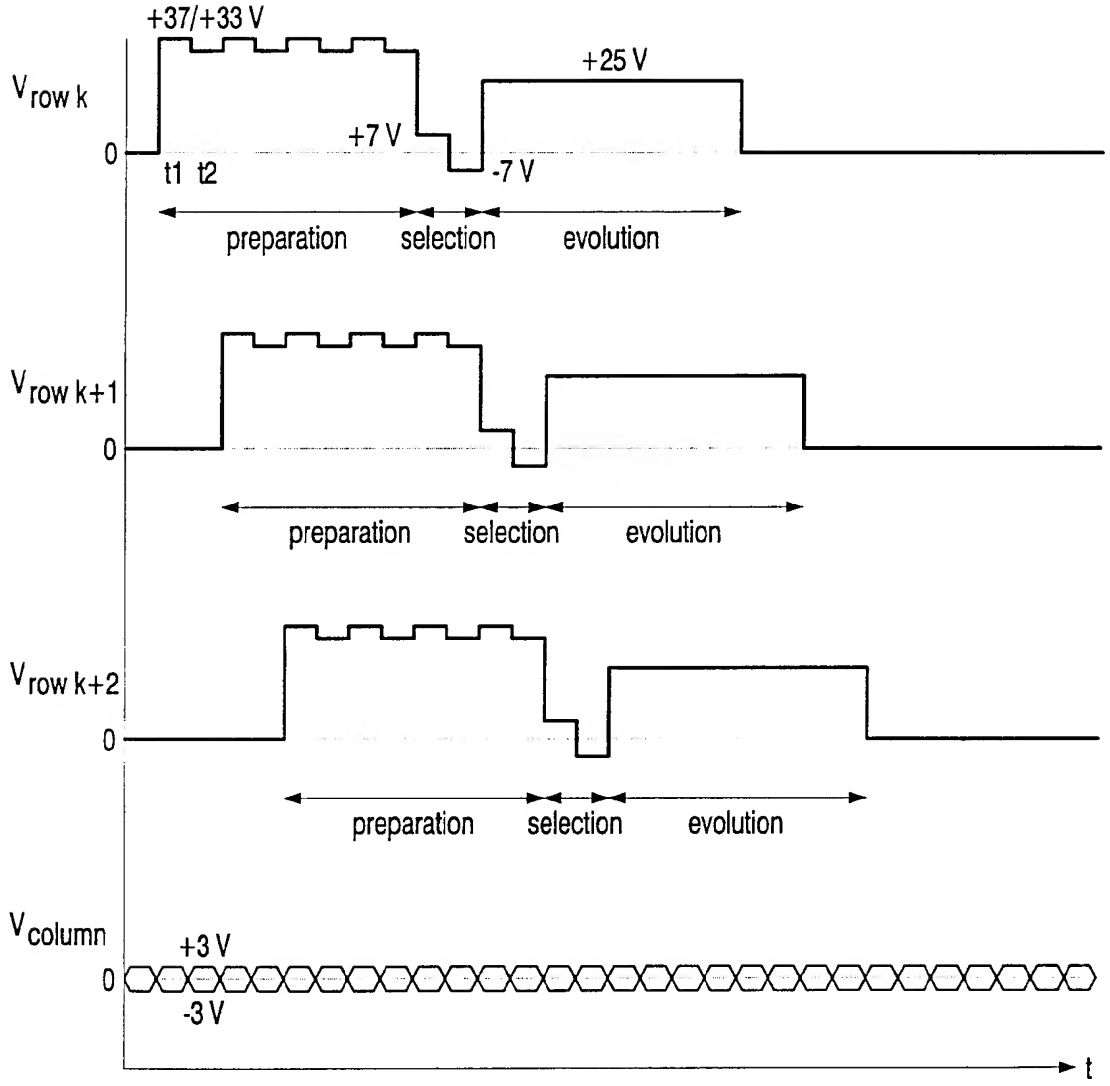
+37/+33 V
+25 V
V row k
+7 V
0
t1 t2
-7 V
preparation
selection
evolution
V row k+1
0
preparation
selection
evolution
V row k+2
0
preparation
selection
evolution
V column
+3 V
0
-3 V
t

FIG. 14

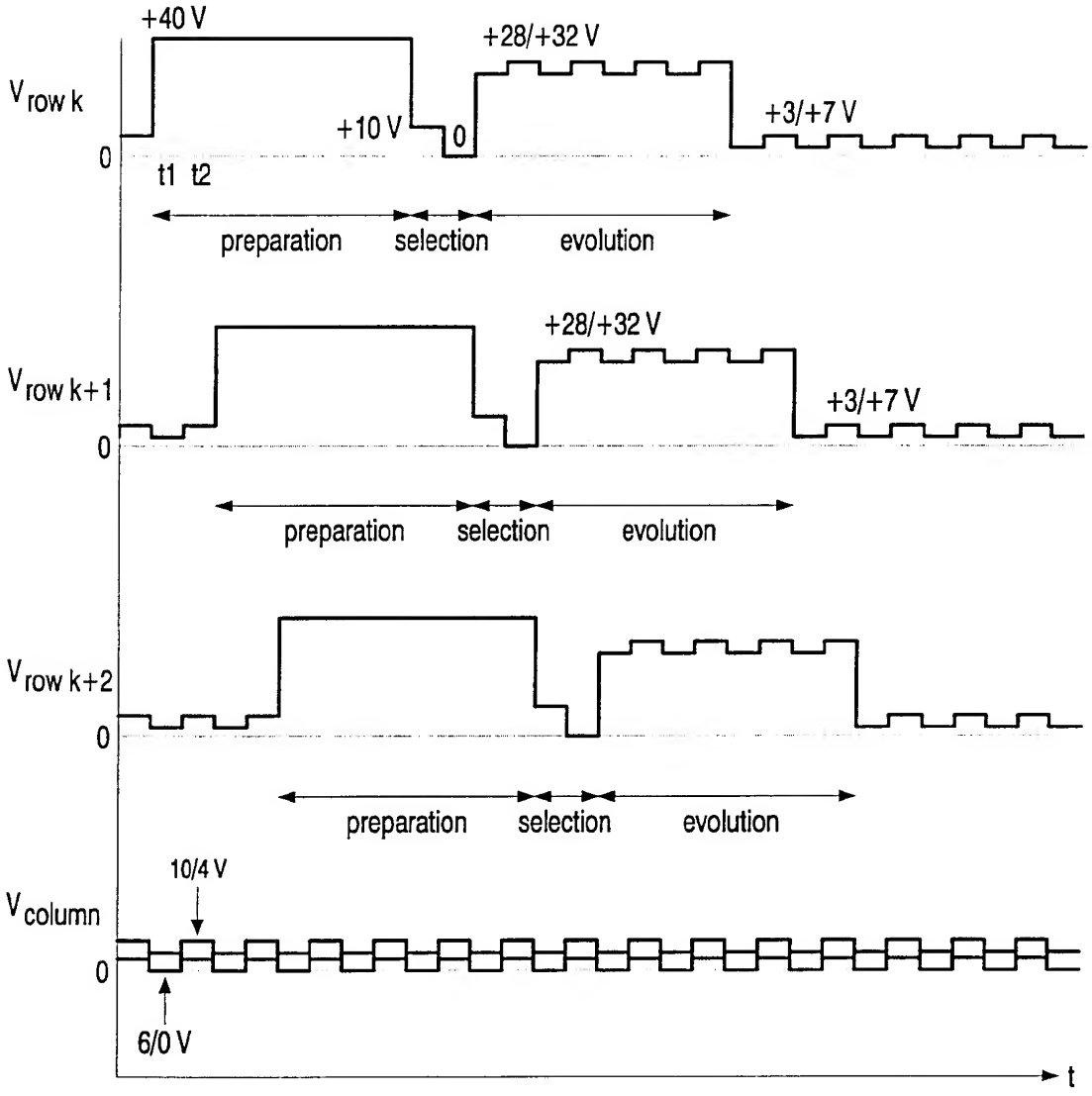
+40 V
+28/+32 V
V row k
+10 V
0
+3/+7 V
0
t1 t2
preparation
selection
evolution
+28/+32 V
V row k+1
+3/+7 V
0
preparation
selection
evolution
V row k+2
0
preparation
selection
evolution
10/4 V
V column
0
6/0 V
t

FIG. 15

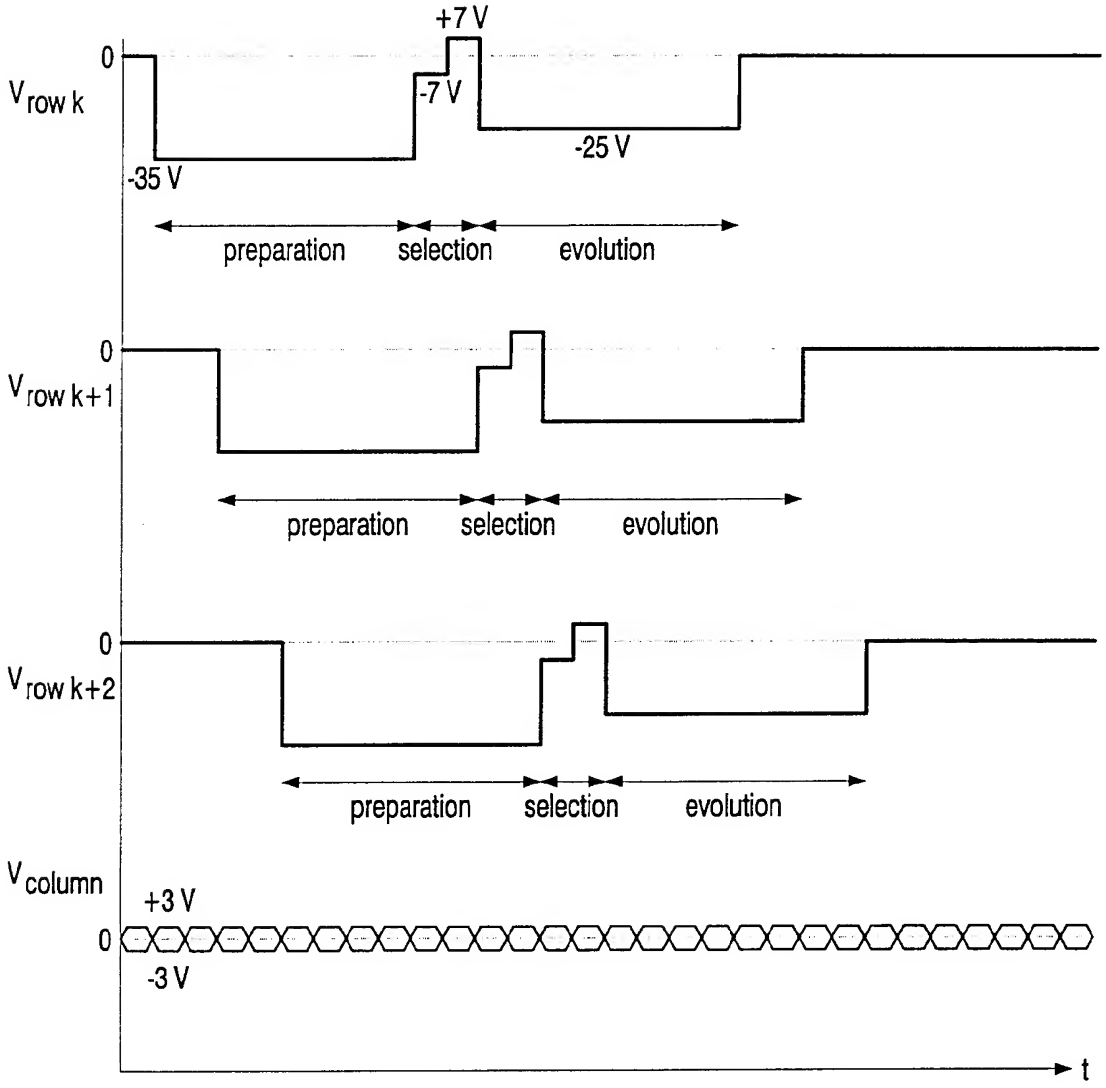
+7 V
0
V row k
-7 V
-25 V
-35 V
preparation
selection
evolution
0
V row k+1
preparation
selection
evolution
0
V row k+2
preparation
selection
evolution
V column
+3 V
0
-3 V
t

FIG. 16

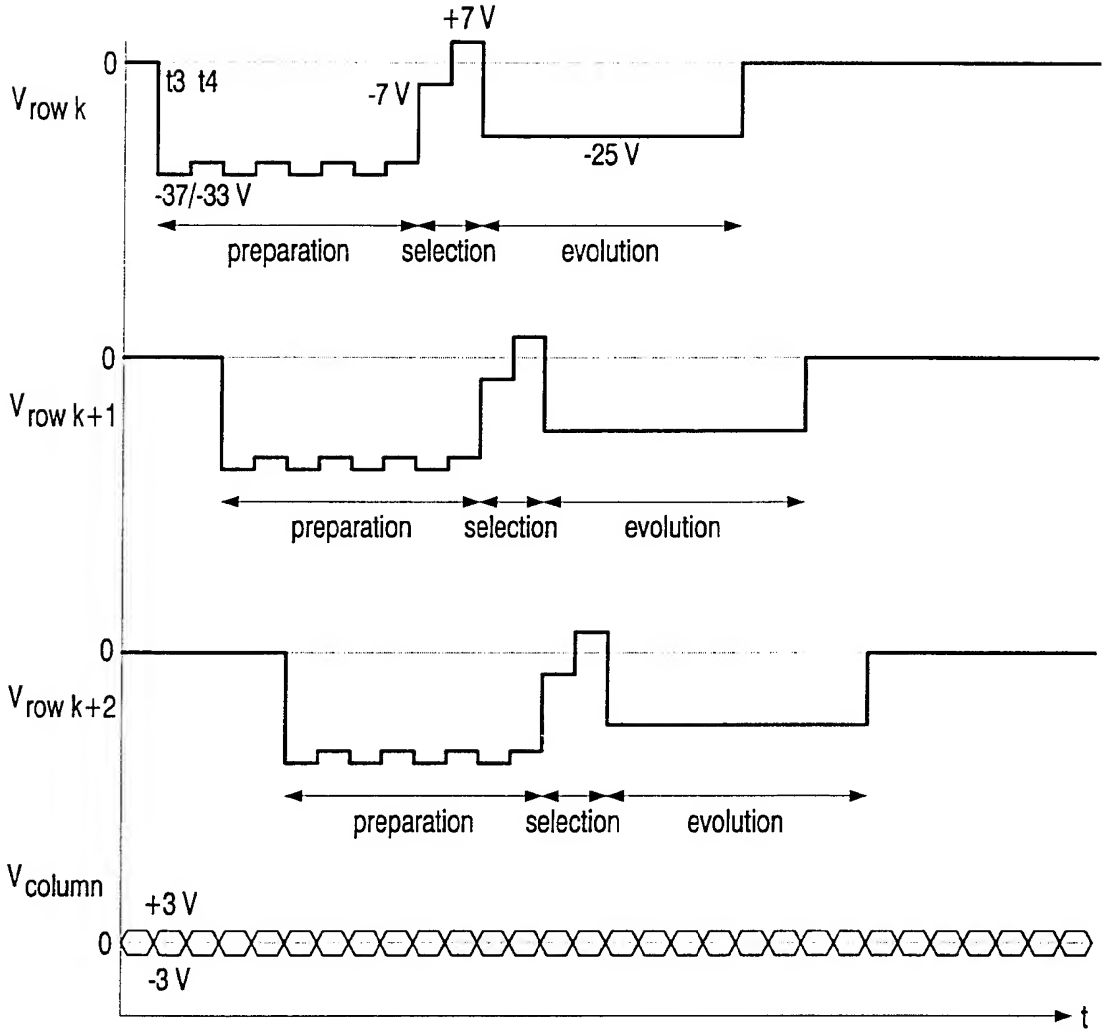
+7 V
0
t3 t4
-7 V
$V_{row\ k}$
-25 V
-37/-33 V
preparation
selection
evolution
0
$V_{row\ k+1}$
preparation
selection
evolution
0
$V_{row\ k+2}$
preparation
selection
evolution
V_{column}
+3 V
0
-3 V
t

FIG. 17

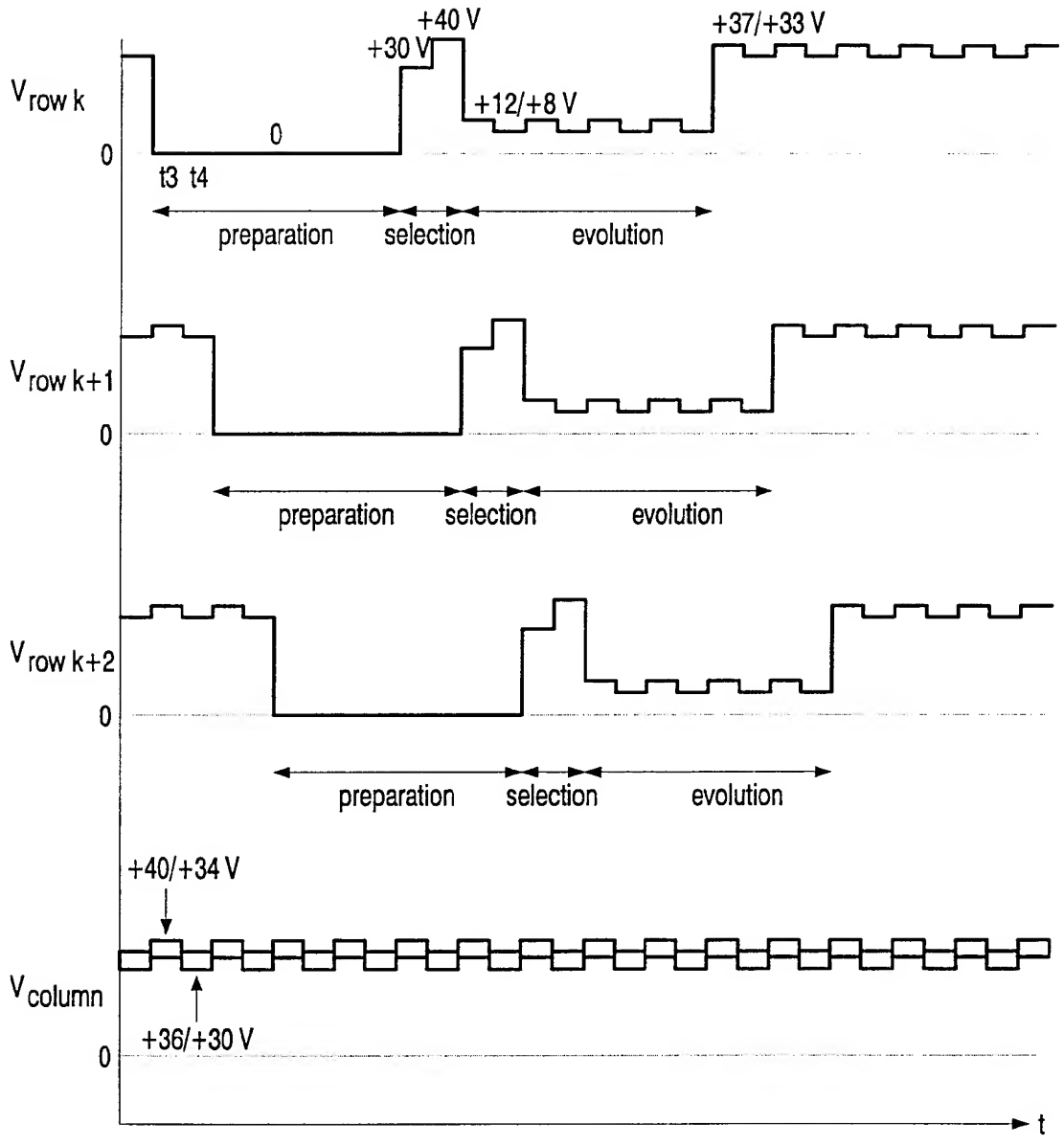
+40 V
+30 V
+37/+33 V
+12/+8 V
V row k
0
0
t3 t4
preparation
selection
evolution
V row k+1
0
preparation
selection
evolution
V row k+2
0
preparation
selection
evolution
+40/+34 V
V column
+36/+30 V
0
t

FIG. 18

INTERNATIONAL SEARCH REPORT

Intern: ıal Application No
PCT/EP 00/06684

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G09G3/36

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	HUANG X -Y ET AL: "36.3: UNIPOLAR IMPLEMENTATION FOR THE DYNAMIC DRIVE SCHEME OF BISTABLE REFELECTIVE CHOLESTERIC DISPLAYS" , SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS,US,SANTA ANA, SID, VOL. VOL. 28, PAGE(S) 899-902 XP000722835 ISSN: 0097-966X the whole document	1-7

☐ Further documents are listed in the continuation of box C.

☐ Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 October 2000	03/11/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Amian, D

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